REMARKS

Claim 13 is amended, no claims are canceled, and no claims are added; as a result, claims 13-16 and 32-60 are now pending in this application.

The Office Action states

> Since the disclosure never supported this feature prior to the proposed Figure 6, stating that this feature is equivalent to an admission that a DRAM containing its own row decoder, column decoder data in buffer and data out buffer was prior art.

Applicant has made no such admission. Applicant requests legal support for the examiner's assertion.

The Office Action further states that a submission in a co-pending is further evidence that applicant concedes that this feature was prior art. Applicant does not and has not conceded that this feature was prior art. Moreover, applicant is unsure of how features are prior art. Prior art is defined by 35 USC 102 and applicant can not find where 35 USC 102 mentions features.

Double Patenting Rejection

Claims 13-16 and 32-60 were rejected under the judicially created doctrine of double patenting as being unpatentable over claims 1-4, 26-28 and 32-57 of U.S. Patent No. 6,286,062. Claims 13-16 and 32-60 were provisionally rejected under the judicially created doctrine of double patenting as being unpatentable over claims 50-54 of U.S. Application No. 09/434,731 (now issued as U.S. Pat. No. 6,418,495). Applicant herewith submits a Terminal Disclaimer to overcome these rejections.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§103 Rejection of the Claim

Claims 13-16 and 32-60 were rejected under 35 USC § 103(a) as being unpatentable over Katayama et al.(U.S. Patent No. 5,875,452) in view of Rosich et al. (U.S. Patent No. 5,587,964). Applicant traverses.

With regard to claim 13, it recites, in part, "wherein a first load on the command and address bus is equal to N devices and a second load on the data bus is equal to N devices where the total number of memory devices is N*M." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 13 is allowable.

With regard to claim 32, it recites, in part, "wherein the socket couples the memory module to a unidirectional command and address bus and to a bidirectional data bus . . ." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 32 is allowable.

With regard to claim 34, it recites, in part, "inserting the memory module in the socket; communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus" and "communicating the data, through the socket to a memory controller, on the bidirectional data bus." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 34 is allowable.

With regard to claim 36, it recites, in part, "a connector, wherein the connector includes command and address lines coupled to the first register and data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 36 is allowable.

With regard to claims 40 and 42, each recites, in part, "coupling the connector to the socket". ." The Office Action does not indicate where the examiner finds this feature in

Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claims 40 and 42 are allowable.

With regard to claim 44, it recites, in part, "wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 44 is allowable.

With regard to claims 48 and 52, each recites, in part, "communicating the data, through the socket to the memory controller, on a bidirectional data bus." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claims 48 and 52 are allowable.

With regard to claim 52, it recites, in part, "a plurality of N memory modules, wherein each of the memory modules includes: a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer" and "wherein each of the command and address bus and the data bus support N*M memory devices and only experience a load of N registers." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 52 is allowable.

With regard to claim 56, it recites, in part, "a connector, wherein the connector includes command and address lines coupled to the second register and data lines coupled to the first register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus." The Office Action does not indicate where the examiner finds this feature in Katayama et al. or Rosich et al. Accordingly, applicant submits that a prima facie case of obviousness has not been made and that claim 56 is allowable.

The dependent claims not specifically addressed above are believed to be allowable at because they depend from an allowable independent claim.

Moreover, the examiner admits that Katayama et al. does not specifically mention a data in and a data out buffer (Office Action page 5). It appears that the examiner is relying on his statement that adding additional levels of buffer hierarchies was well known at the time the invention was made to read elements into Katayama that it does not teach. Applicant respectfully traverses this assertion as a form of official notice as the examiner is relying on his assertion that adding levels of buffer hierarchies was well known at the time the invention was made. Applicant requests that the examiner provide a reference that describes such an element. Absent a reference, it appears that the examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

The examiner further admits that Katayama et al. and Rosich et al. do not specifically mention that memory controller 17 could be connected to more than one memory storage device 16. The embodiments presently claimed include, in part, a plurality of N memory modules, wherein each of the memory modules includes: a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Applicant respectfully submits that the examiner's reliance on the his belief that adding the additional buffers was well known actually is hindsight. The examiner has not applied any reference that shows all of the features of the present claims. As all of the features are not shown in Katayama et al. or in Rosich et al., applicant submits that the pending claims are allowable.

The examiner states that several storage device 16 in parallel would have allowed for faster data retrieval via parallel data transfers. If a plurality of Katayama et al.'s memory systems were connected to it bus, then it would have the same drawback as described in the present application for conventional memory systems. That is, the load on the buses would be the number of memory devices times the number of memory systems connected to the bus. In contrast, the present invention adds a buffer to each memory system so that the load on the bus is

equal to the number of memory systems not the number of memory devices times the number of memory systems. Accordingly, there is no expectation of success in modifying Katayama to arrive at the presently claimed invention.

The Office Action further relies on St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977) for a position that duplicate parts for multiple effects is not given patentable weight. Applicant does not see how St. Regis Paper applies to the present claims. First. Applicant requests that the "duplicate parts" relating to the present claims be identified. It appears that the examiner believes adding multiple storage devices 16 of Katayama et al. teaches all of the elements recited in the claims. Applicant respectfully traverses. Specifically, merely adding a plurality of Katayama's storage devices together does not teach or even suggest all of the elements of the claims. Specifically, Katayama does not teach or suggest the pipelined memory subsystems that each have a plurality of memory devices, wherein each contains a data in and a data out buffer, a column decoder and a row decoder, a first register and a second, data register as recited in claim 13. Further, the elements as recited in claim 13 do not rely on merely duplicating parts such as paper bag layers. The present invention as defined by claim 13 includes a plurality of memory subsystems, each connected to a controller through a command and address bus and a data bus. Each of the memory subsystems includes a plurality of memory devices, a command register and a data register. The system of claim 13 does not rely only multiple memory subsystems to distinguish over the art. The present system uses a unidirectional C/A bus and a data bus yet supports a plurality of devices per bus such that the total width of the data path width is not cost prohibitive to manufacture. For example, the present invention provides a memory system which utilizes a single 16-bit data bus which can be operated at 800 MHz and which supports 64 devices. Such a system can also be implemented as a higher bandwidth multiple data bus system as described in the specification. Accordingly, the present invention achieves effects beyond merely duplicating the memory systems. Thus, the corresponding address register and data register result in an effect greater than the sum of the several effects taken separately. For example and as illustrated in Figure 1 of the present application memory system 100 comprises N command and address registers 131, N data registers and N*M DRAMS. Each command and address buffer drives the latched command

and address information to its corresponding plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices. Additionally, the load on data bus 120 is reduced from N*M devices to only N devices. As a result the effects of the data in and data out buffer of each of the plurality of memory devices, in combination with the address register and the data register within the memory system are more than the sum of the single effects of the internal components of each of the plurality of memory devices. The addition of an address register coupled between a corresponding plurality of memory devices and a unidirectional command and address bus and a data register coupled between the corresponding plurality of memory devices and a bidirectional data bus results in an embodiment of the present memory system that uses a single 16-bit data bus which can be operated at 800 MHZ and which supports 64 devices. In sum, the present invention as defined by the claims is not obvious under §103. And is certainly not analogous to the courts resolution in St. Regis interpretation of redundancy which found merely adding layers to a paper bag was obvious. Reconsideration is requested.

Telephone Interview Request

The undersigned requests a telephone interview with the examiner as the undersigned believes that such an interview would assist in resolving the issues in this application. Please call the undersigned at 612-349-9587 at the examiner's convenience.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KEVIN J. RYAN

By his Representatives,

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Date 26 June '03

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26th day of June, 2003

Amy Moriarty
Name

Signature